Low Cost High Performance Mono Audio DAC

FEATURES

- High performance and low power multi-bit delta-sigma audio DAC
- 110 dB signal to noise ratio, -85 dB THD+N
- 24-bit, 8 to 48 kHz sampling frequency
- Differential output
- I^2S slave serial data port
- 32/64/128/256Fs system clocks
- 1.8V to 3.3V operation

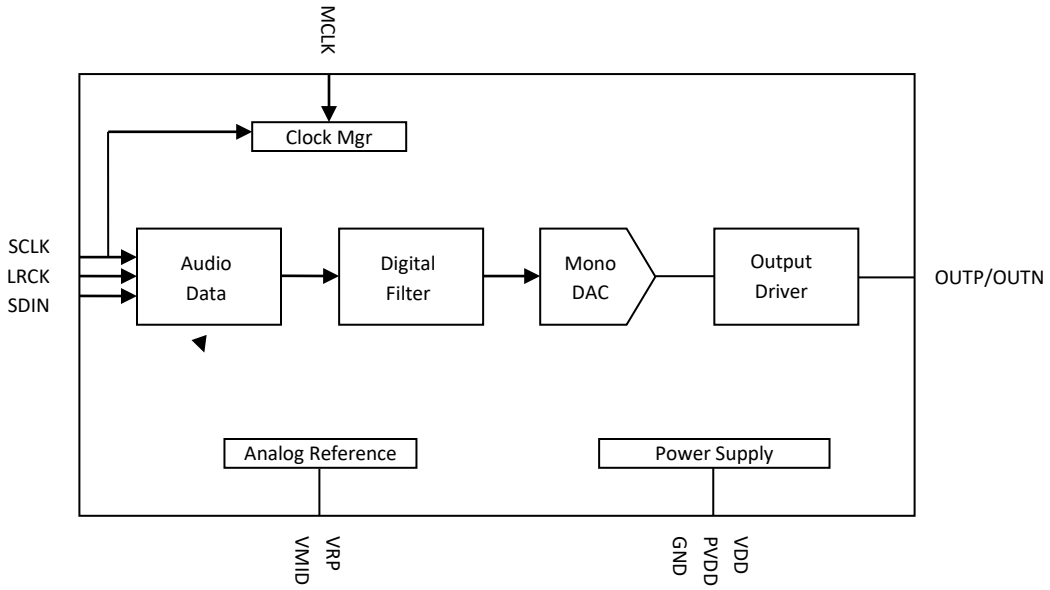
APPLICATIONS

- Cloud speaker
- Voice or audio playback

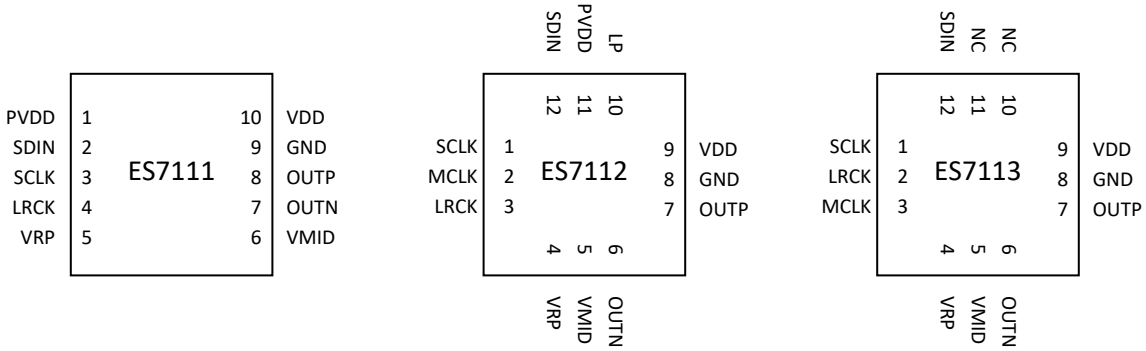
ORDERING INFORMATION

ES7111/2/3 -40°C ~ +85°C
ES7111 DFN-10
ES7112 QFN-12
ES7113 QFN-12

1 BLOCK DIAGRAM

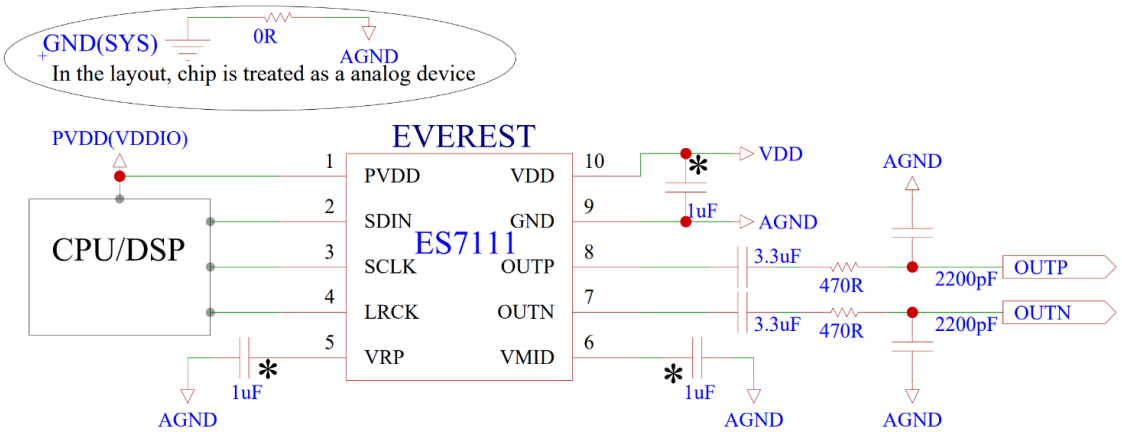


2 PIN OUT AND DESCRIPTION

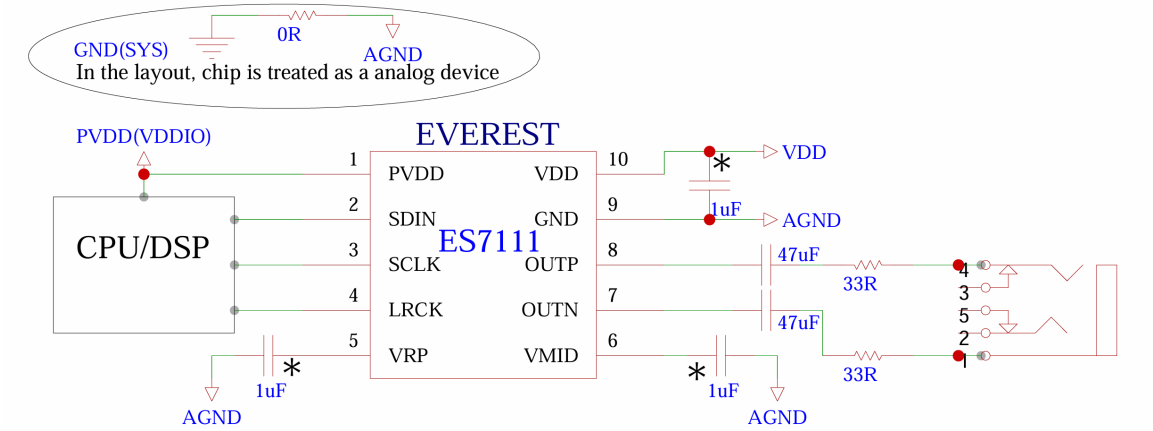


Pin Name	ES7111 Pin number	ES7112 Pin number	ES7113 Pin number	Input or Output	Pin Description
PVDD	1	11		Analog	Power supply for the digital input and output
SDIN	2	12	12	I	DAC serial data input
SCLK	3	1	1	I	Serial data bit clock
MCLK		2	3	I	Master clock
LRCK	4	3	2	I	Serial data left and right channel frame clock
VMID VRP	6 5	5 4	5 4	Analog	Filtering capacitor connection
OUTN OUTP	7 8	6 7	6 7	Analog	Differential analog output
GND VDD	9 10	8 9	8 9	Analog	Power supply
LP		10		I	Set high for sampling frequency above 25 kHz Set low for sampling frequency below 25 kHz

3 TYPICAL APPLICATION CIRCUIT



✻ For the best performance,decoupling and filtering capacitors should be located as close to the device package as possible



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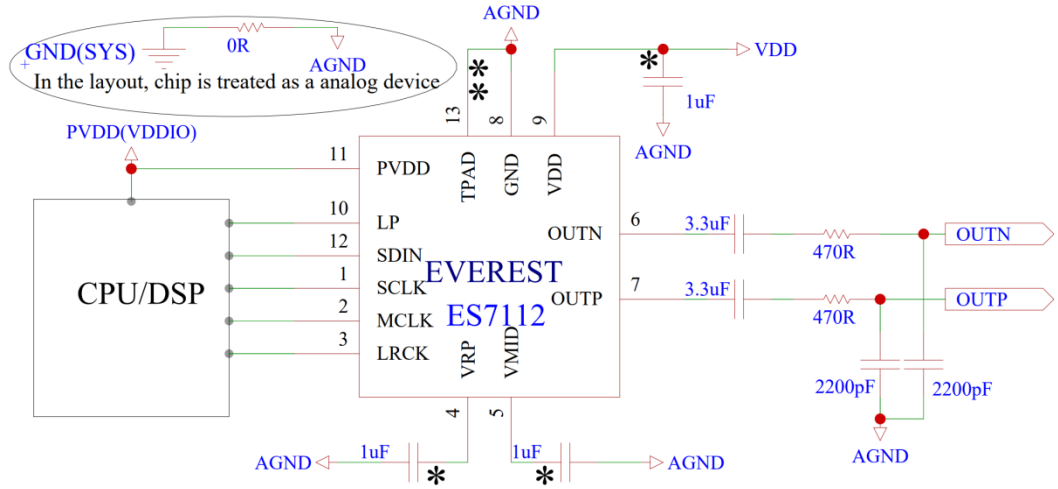
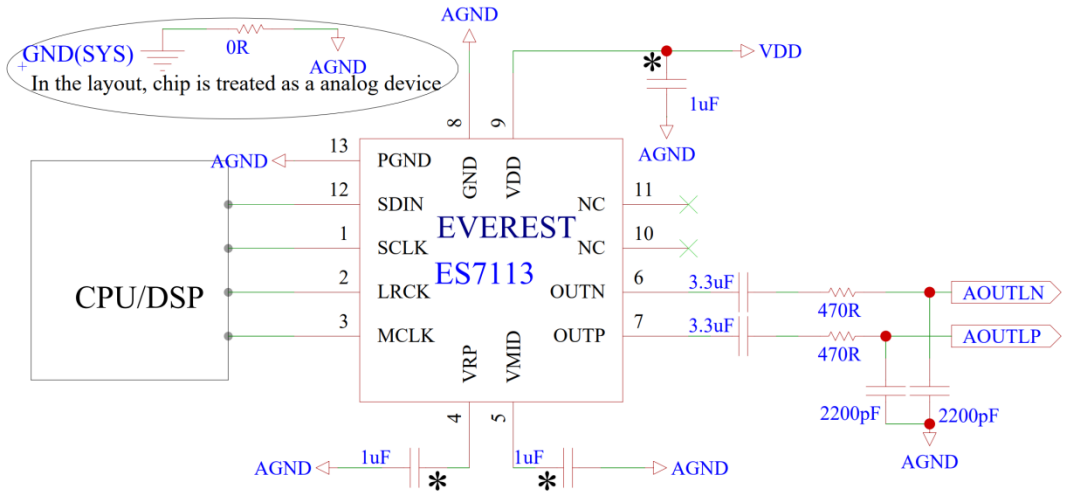


✻ For the best performance,decoupling and filtering capacitors should be located as close to the device package as possible
✻✻ PIN13:TPAD(Thermal PAD) must be connected to PIN8:GND



✻ For the best performance,decoupling and filtering capacitors should be located as close to the device package as possible

4 CLOCK MODES AND SAMPLING FREQUENCIES

LRCK and SCLK are supplied externally. LRCK and SCLK must be synchronously derived from the system clock with some specific rates. The device can auto detect MCLK/LRCK ratio according to Table 1. The device only supports the MCLK/LRCK ratios listed in Table 1. For ES7111, SCLK is used as MCLK.

Table 1 Slave Mode Sampling Frequencies and MCLK/LRCK Ratio

Sampling Frequency	MCLK/LRCK Ratio
8kHz – 32kHz	32, 48, 64, 96, 100, 125, 128, 192, 250, 256, 320, 384, 400, 500, 512, 640, 750, 768, 1024, 1152, 1280, 1536, 2048, 2304, 3072
44.1kHz – 48kHz	32, 64, 125, 128, 192, 250, 256, 320, 384, 500, 512, 640, 750, 768, 1024

5 DIGITAL AUDIO INTERFACE

The device supports I^2S serial audio data interface through LRCK, SCLK and SDIN pins. SDIN is sampled by the device on the rising edge of SCLK. The relationship of SDATA (SDIN), SCLK and LRCK is shown through Figure 1. Mono data must be in left channel.

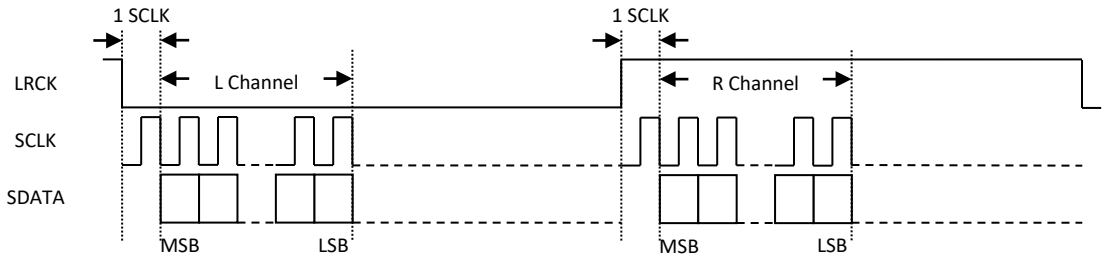


Figure 1 I^2S Serial Audio Data Format

6 ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Continuous operation at or beyond these conditions may permanently damage the device.

PARAMETER	MIN	MAX
Analog Supply Voltage Level	-0.3V	+3.6V
Digital Supply Voltage Level	-0.3V	+3.6V
Digital Input Voltage Range	GND-0.3V	PVDD+0.3V
Operating Temperature Range	-40°C	+85°C
Storage Temperature	-65°C	+150°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	TYP	MAX	UNIT
VDD	2.97	3.3	3.6	V
PVDD	1.6	1.8/3.3	3.6	V

DAC ANALOG AND FILTER CHARACTERISTICS AND SPECIFICATIONS

Test conditions are as the following unless otherwise specify: VDD=3.3V, GND=0V, Ambient temperature=25°C, Fs=48 KHz, MCLK/LRCK=256. For ES7111, SCLK is used as MCLK.

PARAMETER	MIN	TYP	MAX	UNIT
DAC Performance				
Signal to Noise ratio (A-weigh)	105	110	115	dB
THD+N	-90	-85	-80	dB
Channel Separation (1KHz)	105	110	115	dB
Filter Frequency Response				
Passband	0		0.4535	Fs
Stopband	0.5465			Fs
Passband Ripple			±0.05	dB
Stopband Attenuation	53			dB
Analog Output				
Full Scale Output (differential P and N)	1.71*AVDD/3.3	2*0.9*AVDD/3.3	1.89*AVDD/3.3	Vrms
Minimum Load Resistance		33		Ω
Maximum Load Capacitance		100		pF

DC CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT
Normal Operation Mode				
PVDD=1.8V, VDD=3.3V (48 KHz) (Note) PVDD=3.3V, VDD=3.3V (48 KHz)		13 8		mW
Power Down Mode				
PVDD=1.8V/3.3V, VDD=3.3V		0		uA
Digital Voltage Level				
Input High-level Voltage	0.5*PVDD 1.6 (ES7113)			V
Input Low-level Voltage			0.5	V

Note: turn on PVDD before VDD and turn off PVDD after VDD, or turn on or off PVDD and VDD within 10 ms of each other.

SERIAL AUDIO PORT SWITCHING SPECIFICATIONS

PARAMETER	Symbol	MIN	MAX	UNIT
MCLK frequency			49.2	MHz
MCLK duty cycle		40	60	%
LRCK frequency			50	KHz
LRCK duty cycle		40	60	%
SCLK frequency			26	MHz
SCLK pulse width low	T_{SLKL}	16		ns
SCLK Pulse width high	T_{SCLKH}	16		ns
SCLK falling to LRCK edge (master mode only)	T_{SLR}		10	ns
LRCK edge to SCLK rising (slave mode only)	T_{LSR}	10		ns
SDIN valid to SCLK rising setup time	T_{SDIS}	10		ns
SCLK rising to SDIN hold time	T_{SDIH}	10		ns

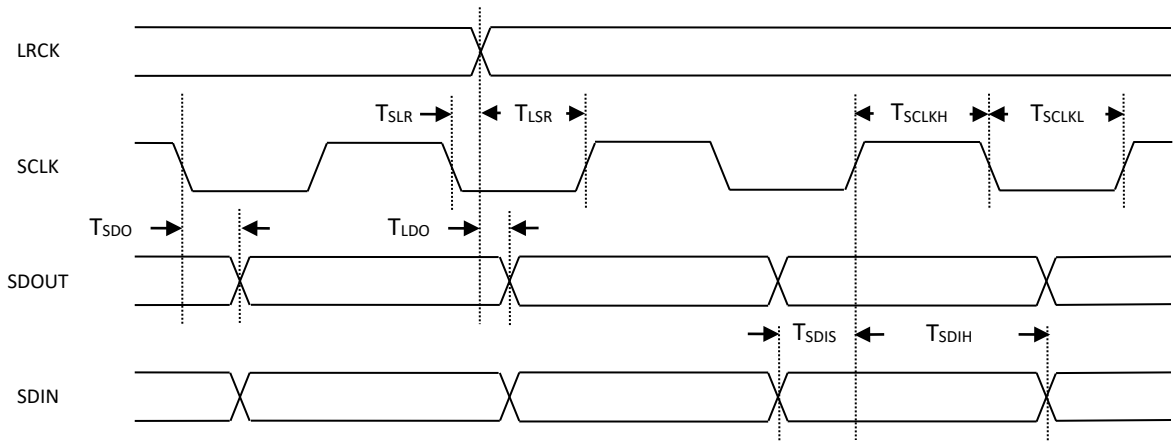
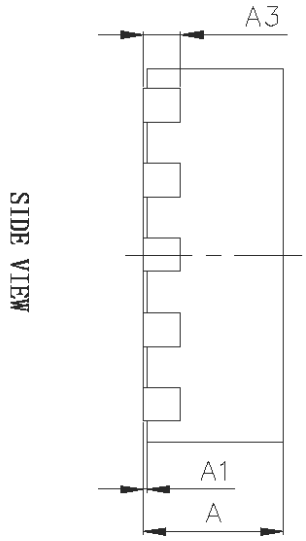
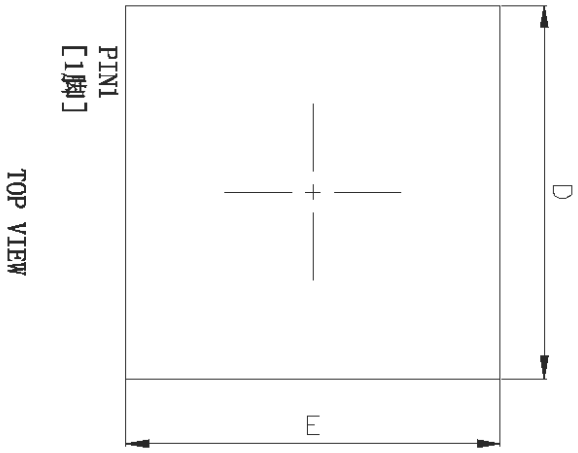


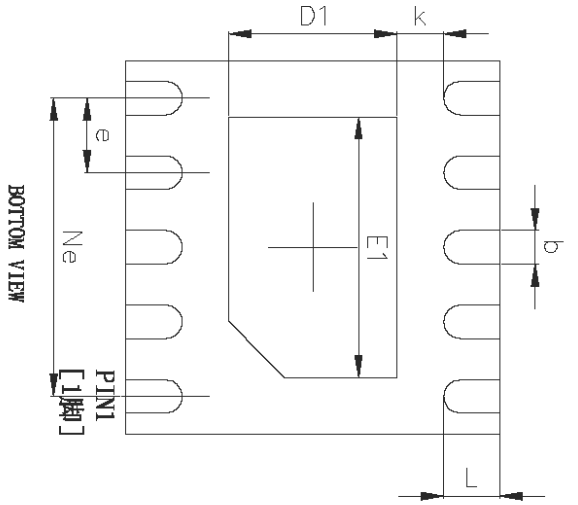
Figure 2 Serial Audio Port Timing

7 ES7111 PACKAGE (UNIT: MM)

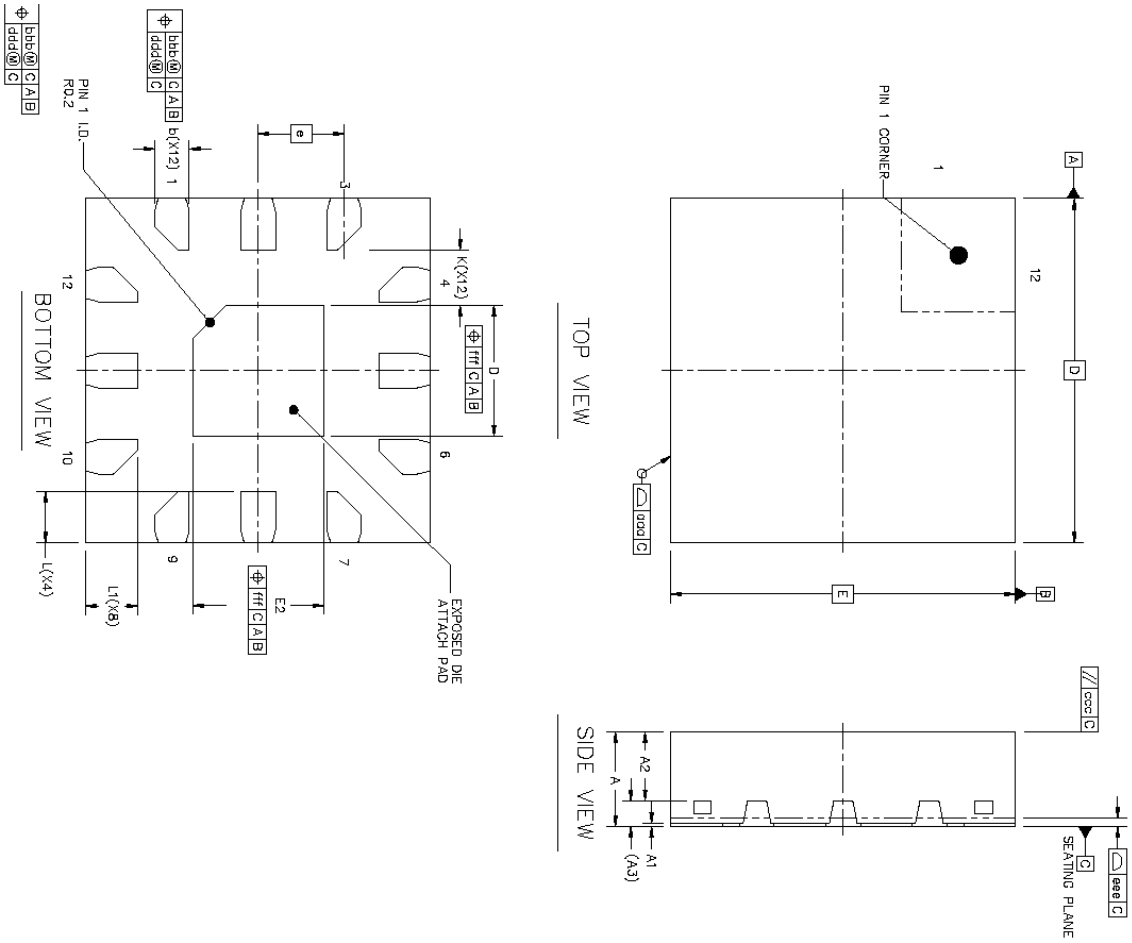




SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.700	0.750	0.800
A1	0.000	0.025	0.050
A3		0.203REF.	
D	1.900	2.000	2.100
E	1.900	2.000	2.100
D1	0.800	0.900	1.000
E1	1.300	1.400	1.500
k		0.250REF.	
b	0.155	0.180	0.205
e		0.400BSC	
Ne		1.600BSC	
L	0.250	0.300	0.350

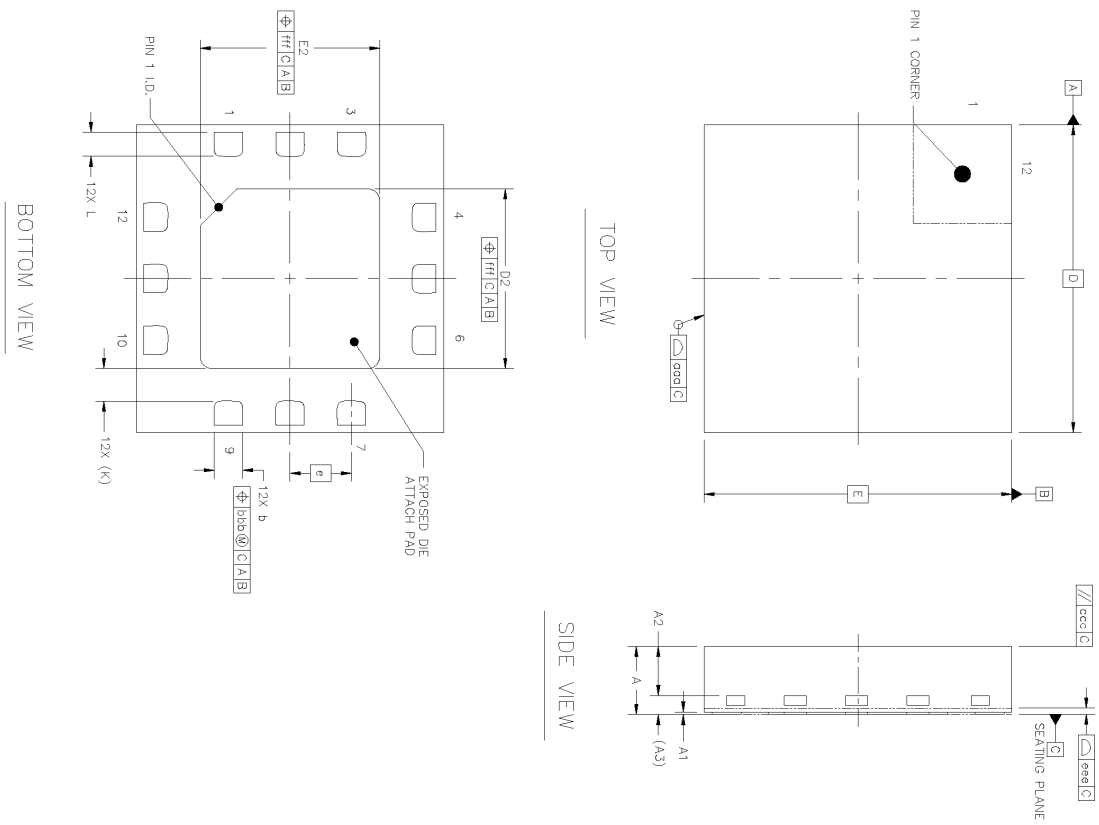


8 ES7112 PACKAGE (UNIT: MM)



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.5	0.55	0.6
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.4	---
L/F THICKNESS		A3		0.152 REF	
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D		2 BSC	
	Y	E		2 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	D2	0.66	0.76	0.86
	Y	E2	0.66	0.76	0.86
LEAD LENGTH		L	0.25	0.3	0.35
		L1	0.2	0.3	0.4
LEAD TIP TO EXPOSED PAD EDGE		K		0.32 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.05	
LEAD OFFSET		bbb		0.1	
		ddd		0.05	
EXPOSED PAD OFFSET		fff		0.1	

9 ES7113 PACKAGE (UNIT: MM)



	SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS	A	0.5	0.55	0.6
STAND OFF	A1	0	0.02	0.05
MOLD THICKNESS	A2	---	0.4	---
L/F THICKNESS	A3		0.152 REF	
LEAD WIDTH	b	0.18	0.23	0.28
BODY SIZE X	D		2.5 BSC	
BODY SIZE Y	E		2.5 BSC	
LEAD PITCH	e		0.5 BSC	
EP SIZE X	D2	1.36	1.46	1.56
EP SIZE Y	E2	1.36	1.46	1.56
LEAD LENGTH	L	0.1425	0.1925	0.2425
LEAD TIP TO EXPOSED PAD EDGE	K		0.265 REF	
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	ccc		0.1	
COPLANARITY	eee		0.05	
LEAD OFFSET	bbb		0.1	
EXPOSED PAD OFFSET	fff		0.1	

NOTES
1.REFER TO JEDEC MO-220;
2.COPLANARITY APPLIES TO LEADS, CORNER LE

10 CORPORATE INFORMATION

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